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Technology Trends and Design Aspects of Data Processing Cores of Future Small Smart Objects

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Abstract What will be the function and structure of intelligence of small, even invisible, smart objects, what kind of development efforts must be done before this kind of small smart objects are possible, and what are the conceptual design and implementation choices available now? This paper assumes that the limit between the feature size of visible and invisible object is approximately 0.2 mm. It shows that scalable CMOS technology is capable to perform the needed logic operations in small objects to the level of human cell size but not down to the virus-sized nanorobot level. Here is stated that the most suitable digital electronics computing structure of a smart small object is the structure capable to perform reconfigurable computing instead of a fixed logic structures.

Keywords Reconfigurable computing · swarm intelligence ·

1 Introduction

"There's Plenty of Room at the Bottom" said Richard P. Feynman in his classic visionary talk that he gave on December 29th 1959 at the annual meeting of the American Physical Society [1]. Feynman assumed in his talk that if the resolving power of the human eye is about 0.2 of a millimeter, the diameter of the head of a pin is 1.6 mm and the text could be de-magnified by 25,000 times, then there will be enough room on the head of a pin to put on it all of the *Encyclopaedia Brittanica*. Still after the de-magnification, the smallest dots of the text are 8 nm across and cover the area of 1000 atoms, each. The surface area of a pin is approximately 8 square millimeters.

J. Storrs Hall has created a vision of the stuff consisting of a swarm of small smart objects, nanorobots. He called it *Utility Fog*. In this Hall's concept nanorobots, *Foglets*, each has twelve arms, arranged as the faces of a human cell sized dodecahedron. [2]

Bruce R. Donald's group has reported the smallest controllable untethered robot with dimensions 60 μm by 250 μm by 10 μm [3]. It receives a common power and control signal trough a capacitive coupling with an underlying electrical grid. The control information received through the grid is stored as electromechanical state information on-board the robot. The intelligence of this robot is restricted to an electro-mechanical control system which is analogous to a digital four-state finite state machine.

Fig.1 shows relative sizes of biological objects compared to the human made objects.

The mean length of a bacterium is something like 1 μm and that of a human cell 10 μm. The DNA in a given bacterium is capable to hold about a megabyte of information, and that in a human cell about a gigabyte [2 p. 110]. Requicha defines in [9] that nanosystems are objects with overall sizes on the order of a few micrometers or less in all three spatial directions. Following this definition, one could say that nano-level smart objects, e.g., nanorobots have dimensions similar to a human cell and a bacterium. A biological virus has even smaller dimensions, few ten's of nanometers.

The semiconductor industry has moved lately to use 65 nm feature size in integrated circuit manufacturing. 45 nm level of the wire wide is coming in to use soon and 22 nm can be reached during the first half of the next decade. ITRS Road Map for semiconductors estimates that 14 nm feature sizes are possible in 2020 [8]. At present, the wide of a metal or poly wire (65 nm) on the surface of an integrated circuit has the size comparable to that of an ordinary biological virus.

There are several possibilities to utilize the small feature sizes of integrated electronics offered by the modern semiconductor industry. We can implement one function as efficiently as possible in each chip in the system, we can put several function on one chip to implement System-on-a-Chips (SoC) or Network-on-a-Chips (NoC) , or we can use huge number of small, even invisible, identical chips and put them to work together.

A major obstacle facing nanotechnology today is the lack of effective processes for building the nanoscale structures. We do need nanotechnology for its ability to manufacture high-tech items in astronomical quantities needed by the envisaged applications. On the other hand, nanotechnology is not needed before one is able to start designing and experimenting with nanoscale hardware objects and software. In this paper experimental design cases of macro models of computing structures suitable for visible, and even invisible, objects are described.

Programming and configuring swarms of smart objects, nanorobots in the future, is a research area with strong connections with several emerging fields of computer science and digital and analog electronics: sensors/actuator networks, distributed robotics, and swarm intelligence.

The remainder of this paper will proceed as follows. Chapter 2 gives some background facts to the issue. Chapter 3 describes practical system design aspects and limitations to be encountered in smart object population implementations. Chapter 4 gives visions of possible applications of small smart object systems.

2 Background facts

2.1 From macro-scale to nano-scale

Following milestones are expected here during the evolution of smart objects' size from macro scale down to real nanorobots.

Macro-scale: Means here smart objects' feature sizes of one centimeter and volumes of approximately one cubic centimeter. This could be the size of hardware units used for emulation of intelligence of swarms and grids of smart objects. The first generation of intelligence of smart small objects in the form of reconfigurable hardware could be considered to be on this size level.

Head of pin scale: Diameter and area of a head of a pin is approximately 1.6 mm and 8 mm^2, respectively. The total area of one thousand of this like units is something like 0.6 square meters. This is practical piece of information needed when one is going to calculate, for instance, how much energy a 0.6 square meters solar cell could produce. Second generation.

Micro-scale/(Invisible): Feature sizes smaller than 200 µm are difficult to see by human eyes. For instance, diameter of a dot used in this text is approximately 0.2 mm. Third generation.

Human cell size scale: Human cells are invisible and the size of them is in the range from 1 µm to 10 µm. Fourth generation.

Real nano-scale: In Nano-scale, 10 nm … 100 nm, individual molecules and even atoms could be manipulated. Fifth generation.

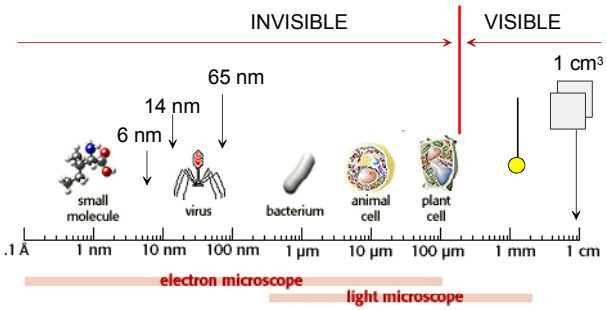

Fig. 1 Relative sizes of small objects [4]

2.2 Data processing chip in smart objects

Usually, it is assumed that the computing core of smart objects could be a digital processor having Von Neumann or Harvard type architecture [2], [4], [5]. Biological cells are different but still like nanorobots [4]. Human beings are constructed of huge number of almost identical cells. They are able to replicate themselves and to reshape to adapt to different purposes by reading instructions written in DNA. The nature has not made the choice of programmable computer architecture.

The number of objects needed to perform useful operations in a nanorobot network could be so big that special care has to be put on selecting the suitable computing hardware architecture. Instead of selecting a certain fixed Von Neumann or Harvard type architecture, a reconfigurable computing structure found in modern FPGA ICs sounds better choice. Reconfigurable structure can be configured to act as Von Neumann type processor core and even its features can be changed during the operation if needed.

Drawback with the FPGA structures available to day is their silicon area inefficiency compared with ASIC technology. FPGA structure occupies nowadays in general 35 times as much silicon area as respective ASIC structure.

We can write

$$A_{fpga} = kA_{asic}\,, \qquad (1)$$

where A_{fpga} and A_{asic} are silicon surface areas of FPGA and ASIC logic, respectively. k is a technology dependent coefficient telling us how much more silicon area is needed to get a digital logic structure configurable compared to a respective fixed implementation.

Figures in the following Table 1 have been derived so that first three lines are taken from ITRS Road Map

Table 1 High Performance MPU and ASIC Road Map

	Year	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	
	Numbers from ITRS Road Map (Tables 1i and 1j)															
	MPU/ASIC Metal 1 (M1) ½ Pitch	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	nm
	Logic Gate (4-transistor) Area	*1,30*	*1,03*	*0,82*	*0,65*	*0,51*	*0,41*	*0,32*	*0,26*	*0,2*	*0,16*	*0,13*	*0,1*	*0,08*	*0,06*	µm2
	Transistor density logic	*357*	*449*	*566*	*714*	*899*	*1133*	*1427*	*1798*	*2265*	*2854*	*3596*	*4531*	*5708*	*7192*	Mtransistors/cm2
VISIBLE	**Chip in a CUBIC CENTIMETER OBJECT**															
	Fixed logic	89	112	142	179	225	283	357	450	566	714	899	1133	1427	1798	MGates/cm2
	Reconfigurable logic	3	3	4	5	6	8	10	13	16	20	26	32	41	51	MGates/cm2
	Chip in a HEAD OF A PIN (square mm)															
	Fixed logic	893	1123	1415	1785	2248	2833	3568	4495	5663	7135	8990	11328	14270	17980	KGates/mm2
	Reconfigurable logic	26	32	40	51	64	81	102	128	162	204	257	324	408	514	KGates/mm2
	NEAR INVISIBLE CHIP(< 200um x 200um)															
	Fixed logic	36	45	57	71	90	113	143	180	227	285	360	453	571	719	KGates
	Reconfigurable logic	1020	1283	1617	2040	2569	3237	4077	5137	6471	8154	10274	12946	16309	20549	Gates
INVISIBLE	**HUMAN CELL SIZE CHIP (10um x 10um = 100 um2)**															
	Switching elements	357	449	566	714	899	1133	1427	1798	2265	2854	3596	4531	5708	7192	Transistors
	Fixed logic	89	112	142	179	225	283	357	450	566	714	899	1133	1427	1798	Gates
	Reconfigurable logic	3	3	4	5	6	8	10	13	16	20	26	32	41	51	Gates
	VIRUS-SIZED NANOROBOTS (<100nm x 100nm)															
	Switching elements	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	Transistors
	Fixed logic	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	Gates
	Reconfigurable logic	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	<1	Gates

Table 2 Number of High-Performance MPUs

Year			2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	
Numbers from ITRS Road Map (Tables 1i and 1j)																	
MPU/ASIC Metal 1 (M1) ½ Pitch			*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	nm
Logic Gate (4-transistor) Area			*1,30*	*1,03*	*0,82*	*0,65*	*0,51*	*0,41*	*0,32*	*0,26*	*0,2*	*0,16*	*0,13*	*0,1*	*0,08*	*0,06*	µm2
Transistor density logic			*357*	*449*	*566*	*714*	*899*	*1133*	*1427*	*1798*	*2265*	*2854*	*3596*	*4531*	*5708*	*7192*	Mtr
Chip in a CUBIC CENTIMETER OBJECT																	
Area factor		1cm2/1cm2	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	cm2
4004	1971	4600 CMOS transistors	78	98	123	155	195	246	310	391	492	620	782	985	1241	1563	x 1000
8086/IBM PC	1978	29000 transistors	12	15	20	25	31	39	49	62	78	98	124	156	197	248	x 1000
Pentium	1993	3,1 Mtransistors	115	145	183	230	290	365	460	580	731	921	1160	1462	1841	2320	x 1
Pentium IV	2003	55 Mtransistors	6	8	10	13	16	21	26	33	41	52	65	82	104	131	x 1
Chip in a HEAD OF A PIN (square mm)																	
Area factor		1 cm2/100	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	*0,01*	
4004	1971	4600 CMOS transistors	776	976	1230	1552	1954	2463	3102	3909	4924	6204	7817	9850	12409	15635	x 1
8086/IBM PC	1978	29000 transistors	123	155	195	246	310	391	492	620	781	984	1240	1562	1968	2480	x 1
Pentium	1993	3,1 Mtransistors	1	1	2	2	3	4	5	6	7	9	12	15	18	23	x 1
Pentium IV	2003	55 Mtransistors	0,06	0,08	0,10	0,13	0,16	0,2	0,3	0,3	0,4	0,5	0,7	1	1	1	
NEAR INVISIBLE CHIP(< 200um x 200um)																	
Area factor		1 cm2/(200 x 200)um2	0,0004	0,0004	0,0004	0,0004	0,0004	0,0004	0,0004	0,0004	0,0004	0,0004	0,0004	0,0004	0,0004	0,0004	
4004	1971	4600 CMOS transistors	31	244	308	388	489	616	776	977	1231	1551	1954	2463	3102	3909	
8086/IBM PC	1978	29000 transistors	5	6	8	10	12	16	20	25	31	39	50	62	79	99	
Pentium	1993	3,1 Mtransistors	0,05	0,06	0,07	0,09	0,1	0,1	0,2	0,2	0,3	0,4	0,5	0,6	0,7	1	
Pentium IV	2003	55 Mtransistors	0,003	0,003	0,004	0,005	0,007	0,008	0,01	0,01	0,02	0,02	0,03	0,03	0,04	0,05	
HUMAN CELL SIZE CHIP (10um x 10um = 100 um2)																	
Area factor		(100 um2)/(1 cm2)	1 ppm														
4004	1971	4600 CMOS transistors	0,08	0,1	0,1	0,2	0,2	0,2	0,3	0,4	0,5	0,6	0,8	1	1	2	
8086/IBM PC	1978	29000 transistors	0,01	0,02	0,02	0,02	0,03	0,04	0,05	0,06	0,08	0,1	0,1	0,2	0,2	0,2	
Pentium	1993	3,1 Mtransistors	0,0001	0,0001	0,0002	0,0002	0,0003	0,0004	0,0005	0,0006	0,0007	0,0009	0,001	0,001	0,002	0,002	
Pentium IV	2003	55 Mtransistors	0,00001	0,00001	0,00001	0,00001	0,00002	0,00002	0,00003	0,00003	0,00004	0,0001	0,0001	0,0001	0,0001	0,0001	
VIRUS-SIZED NANOROBOTS (<100nm x 100nm)																	
Area factor			1E-12														
4004	1971	4600 CMOS transistors															
8086/IBM PC	1978	29000 transistors															
Pentium	1993	3,1 Mtransistors								very small numbers							
Pentium IV	2003	55 Mtransistors															

2006 updated version [8]. Numbers are taken from high-performance forecast. Table has figures concerning five different size levels: Two invisible, two visible, and one between them.

The figures in Table 1 are gate counts. Each column is respecting certain calendar year and expected technology level. Correspondence between year and technology nodes is taken from ITRS Road Map. There are two rows, for fixed and reconfigurable logic, for each object

size groups in Table 1, ten altogether. For example, this year, 2007, one square centimeter chip could contain 89 million fixed logic gates and three million reconfigurable gates. In 2020, if 14 nm manufacturing technology is possible, respective gate counts will be 1.8 giga and 51 million.

The ratio k (Eq. 1) between fixed and reconfigurable logic is assumed in Table 1 to be technology development independent constant 35. In reality, smaller ratio could be achieved. Most of the silicon area of a FPGA chip nowadays is allocated to reconfigurable wiring. Development of new FPGA architectures allow us to make an estimation that the complexity ratio between fixed and reconfigurable logic will be along the years much smaller than 35. In the case of special reconfigurable structures developed just for small objects the area or even volume efficiency could be much more better. That's why the numbers in the Table 1 are quite conservative for reconfigurable logic.

The smallest size group in Table 1, virus-sized nanorobots, is so small that any expected CMOS technology before 2020 can't be used to implement even a single switching element. This means that the intelligence of virus-sized nanorobots has to be implemented using other than conventional scalable CMOS. Probably, same kind of nono-mechanical logic combined with analog behavior could be the solution on that size level.

If the area of one virus-sized chip is 100 nm x 100 nm = 10000 nm^2 and cell area factor for a NAND gate from ITRS Road Map is 320, then the basic cell size of needed manufacturing technology will be 10000 $nm^2/320 = 31.2\ nm^2$. The feature size is a square root of that, approximately 6 nm. This simple calculation imply that the feature size smaller than 6 nm are needed for the technology capable to implement one virus-sized 2-input logic gate.

The first three lines of Table 2 are similar with Table 2. Also the same five size levels are seen. The numbers in Table 2 are number of processors. In every size group, four typical processor cores are listed: 4004, 8086/IBM PC, Pentium and Pentium IV. They are introduced in 1971, 1978, 1993 and 2003, respectively. The number of transistors in every processor core (third column in Table 2) is taken from a table in [10].

We can see from Table 2 that, e. g., 78 000 units of 4004 processor cores can be implemented on a square centimeter chip in 2007 if 68 nm CMOS technology is applied. In other hand, in 2020, if 14 nm CMOS is available, then combination of 10 000 human cell sized smart objects is needed to implement one as powerful core as Pentium IV from the year 2003.

2.3 Power sources

Power is supplied to these machines electrically, optically, or chemically by feeding them some compound. Chemical power tends to be inconvenient because it cannot be easily switched on or off. [9]

2.4 Communication

Communication among small smart objects by means of waves, be they acoustic, electrical, or optical, is likely to be difficult because of the small antenna sizes. If we look at what nature does, we find that bees communicate directly by dancing; ants communicate by releasing chemicals that change the environment; and bacteria also release chemicals, for example, to assess the number of similar bacteria near them.[9]

2.5 Programming/reconfiguring

The smaller object, the bigger amount of them is needed. Only a big swarm of small objects is powerful.

So far the computing architecture of smart object is like stored program computer, we need memory, another silicon chip, for program code.

3. Development of emulation platform for research purposes

Research hypothesis chosen here states: The intelligence of each smart object belonging to the same swarm or breed has to have equal hardware (HW) structure. They mast be capable to perform reconfigurable computing. One object has to be able to copy the reconfiguring bit pattern from the neighboring one. This could be understood to be like cell division in living biological systems.

3.1 First phase of HW development

The first evolution version of intelligence network of smart object swarm's emulation platform is a simple 3D-grid of device sockets for commercial FPGA devices. Sockets are wired together by communication bus. Power, configuration bit-pattern and synchronization signals are fed to the devices through the communication bus.

This first phase platform is used only for emulating the configuration and communication behavior of a swarm of reconfigurable devices. In this phase the objects are not connected to arm, wheels or other robot's functional actuators. Only the behavior of "robots' brains" is investigated.

The size of each smart object is approximately one cubic centimeter in this phase of development.

3.2 Second phase of HW development

Second version of the research platform is a grid of smart objects without power lines. Every individual ob-

ject, in this case only the intelligence core, of the smart object has its own power source. Charging of batteries could be done off-line or by solar-cells.

3.3 Third phase of HW development

The difference of third phase compared to the earlier one is that cells do not form anymore a fixed grid. They are now more like a swarm of freely moving objects. In this third phase different communication options are researched.

Communication channels between separated small cell like objects to be examined, could be, e.g., electro magnetic, magnetic, capacitive coupling, sound and so on. When a swarm has working internal and external communication means, then the individual cells could move freely and be equipped with means of transport and other robot means.

Instead of allowing the objects go freely in relation to each other we are also able to put them together and form brain like reconfigurable computing structure. Volume of one liter could contain one thousand tightly side-by-side located units of cubic centimeter size smart objects. Giga gate reconfigurable structure could be achieved. Head of pin sized cells could form tera-gate structures in same total volume.

3.4 Fourth and plus phases

HW development phases from fourth forward will be trials to put "brain" cells to smaller size. Human cell size smart objects having CMOS logic intelligence may be possible before 2020. Nano machines and other atomic level structures probably replace CMOS logic as the structure of nanorobots' intelligence before 2020.

4. Application visions

Applications of smart objects and the HW structure of the intelligence needed to control them are naturally greatly dependent of the size-category we are dealing with. Visible macro-scale objects could form swarms or grids of thousands of units put together or distributed over application space. Micro- and nano-scale objects could number, instead, millions of units belonging to the same "breed" and working to solve the problems of one specific application. The fantastic property of micro- and nano-scale objects is their capability to fit in a biological or technical construction under investigation.

4.1 Nanotechnological view to applications

Nanotechnology visions forecast that this technology will let us make supercomputers that fit on the head of a pin and fleets of medical nanorobots smaller than a human cell able to eliminate cancer, infections, clogged arteries, and even old age [5], [6], [7]. Ultimate milestone of evolution could be Storrs' *utility fog* and *foglets* [2].

4.2 Central nervous system of smart objects - Megatrend in electronics?

"Fat-ware" trend in electronics represents constructions where electronic systems are implemented by large silicon chips each containing a chip specific function, e.g., memory, data processing core, hardware accelerator and so on. Because of the manufacturing technology needs, operating power of highly integrated silicon chips must be low. System clock frequencies used are on the giga-herz level. When power consumption is approaching the level of 200 W per chip, the electric current driven from 1 volt power supply is approaching 200 amperes. Device packages are large monsters with perhaps thousand pins and massive cooling element on the back. Improvements in this development trend seem to be saturated. Clock frequencies of MCU chips are not increased for several years even if IRTS Road Map forecasts the use of higher clock frequencies to be possible.

Mobile phones are representing "slim-ware" trend in electronics. Instead of putting one function on a single fat chip, everything is put on one or few chips trying to keep the wholeness slim. This leads to SoC or even NoC implementations. The problems encountered in "fat-ware" remains.

Those old development trends do not give changes for many new breakthroughs or even slow progress. A new way to think is needed.

"Thin-ware" or "nano-ware" trend could be the solution to the problems encountered this far. "Nano-ware" trend could be the new megatrend of electronics. Instead of fat chips, SoCs or NoCs the central nervous system of swarms or fleets of small smart objects even nanorobots could be constructed by a huge number of small identical, low power low frequency chips capable to communicate with each other and with the surrounding environment.

4.3 Smart small objects in electronics

Most of the proposed potential applications of nanorobots are expected to be, e.g., in environmental monitoring for microorganisms and in health care [9],[7].

Here are some proposals of smart objects' applications in electronics:

Super computing Swarms of smart objects could be organized to perform tasks needing super computing power. Instead of one or several power hungry computer installations we are able to distribute thousands even millions individual, small and simple, computing elements over the volume where they can communicate

with each others. Perhaps, future supercomputers are invisible!

Multi-tread smart wiring Putting a smart object at both ends of each individual tread in a multi-tread bundle of wires we can implement one wide band wired communication channel. Smart objects, in this application, have to be digital transceivers. Human hair size threads have enough area in their cross section to house a digital transceiver.

Three dimensional imaging 3D reconstruction and manipulation of images are usually done in a central computer or computer farm after the collection of data by means of a specific detector array. A swarm of smart objects could be programmed or reconfigured to do the high definition detection and image reconstruction.

Artificial tracers Instead of radioactive tracers used in flow and other measurement in industry and medicine a float of smart objects could be used to do the job without fear of pollution.

5. Conclusions

An important milestone in the evolution of smart objects is the limit between visible and invisible. The feature size of 0.2 mm is considered here to be the limit between visible and invisible object. Four size categories, generations, of present and future smart small objects are defined here.

The processing core of smart objects will be structure capable to perform reconfigurable computing instead of Von Neumann like stored program architectures.

This paper's view to smart objects is the control logic of them. Four phases of HW development are presented here.

Construction of the central nervous system of large swarms of smart objects in the form of digital reconfigurable logic instead of SoCs and NoCs would be the new megatrend in electronics.

Even 14 nm CMOS technology expected to be available in 2020 is not capable to implement one virus sized NAND gate. 6 nm CMOS technology should be available to implement one virus sized 2-input NAND gate. Probably, 6 nm CMOS technology will never be available. The intelligence of virus sized smart objects should be based on other than CMOS technology. New inventions of nano-scale logic structure should be done.

Emulation of swarm intelligence can be performed by FPGA fixed grids and movable FPGA based smart objects.

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